REMARKS

This application has been reviewed in light of the Final Office Action mailed April 28, 2005. Reconsideration of this application in view of the below remarks is respectfully requested. Claims 1-64 are pending in the application with Claims 1, 7, 18, 21, 26, 27, 32, 42 and 45 being in independent form. By the present amendment, Claims 1, 7, 18, 32, 42 and 58 have been amended. No new matter or issues have been introduced by way of the present amendment.

I. Objection to The Drawings

FIG. 1 has been objected to for having a reference label X36, which is not mentioned in the description. FIG. 1 has been replaced with a replacement sheet omitting the X36 label. However, the dotted line referenced by the X36 label is disclosed in the description. (See: page 22, lines 5-6). FIG. 4 was found to have a similar situation with regards to reference label X20. Therefore, FIG. 4 has been replaced with a replacement sheet omitting the X20 label. However, the dotted line referenced by the X20 label is disclosed in the description. (See: page 28, lines 15-16). Accordingly, Applicant respectfully request withdrawal of the objection to FIG. 1 and FIG. 4.

Additionally, the Drawings have been objected to for allegedly failing to include a reference label for the term "MID" which has been described in the description. However according to the description, MID is an abbreviation for Module Identifying Signal, which is transmitted via module identification wiring 114, as shown in FIG. 2. (See: page 21, lines 8-10). MID is not a structural element, but rather an abbreviation for a particular signal being transmitted across a labeled wiring in FIG. 1 and 2, thus a reference label is not necessary in the drawings. However, it should be noted that FIG. 2 does in fact contain a reference to "MID" in

association with reference label 114. Accordingly, Applicant respectfully request withdrawal of the objection to the drawings.

II. Objection to Claim 58 for Informalities

Claim 58 has been objected to for having a typographical error, specifically, the word "DROM" should be "DRAM". The misspelling has been corrected by way of the present amendment. Accordingly, Applicant respectfully request withdrawal of the objection to Claim 58.

III. Rejection of Claims 1-64 Under 35 U.S.C. §102(e)

Claims 1-64 have been rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,654,270 issued to Osaka et al.

Osaka et al. is focused on a directional coupler in a memory bus, which is formed by a lead line from a controller and a lead line from a memory chip, and contained within a memory module. (See: Abstract of Osaka et al.). More specifically, a motherboard 1 is mounted with a memory controller (MC 10-1) and memory modules 2-2 – 2-9, The motherboard 1 has lines that transfer data between MC 10-1 and the memory chips 10-2 to 10-9 within the memory modules 2-2 to 2-9, as illustrated in FIG. 4 of Osaka et al. and described in column 6, lines 14-18 of the specification. On the motherboard 1, directional couplers C2 to C9 are formed by the main line 1-1 and lines 1-2 to 1-9.

Osaka et al. teaches memory modules using directional coupling (i.e. crosstalk) to communicate between a memory module and a plurality of memory chips. Applicant clearly claims usage of data wiring and not directional coupling to communicate between the memory controller and memory chips. The Examiner's reference to FIG. 3 and 6-7 of Osaka et al. is incorrect as these figures clearly disclose data transmission via directional couplers and not data

wiring. Therefore, Osaka et al., clearly, does not properly anticipate the claims of the present application.

Additionally, Osaka et al. does not teach a relationship between data transmission speeds on lead lines 1-2 to 1-9 and lead lines 20-2 to 20-9. On the other hand, Applicant's claimed invention is clearly directed towards data transmission on a plurality of data wiring being at a higher speed than data transmission on a plurality of internal data wiring. Support for the above is shown in Applicant's FIG. 2 and described on page 22 lines 26-28 of the specification.

Further, Claim 7 recites: "...each of said modules is provided with at least one buffer, and the buffer of each module is connected to the buffer of another module and/or said controller via data wiring for data transmission..." Such a Daisy chained structure is not taught in Osaka et al.

Moreover, because Osaka et al. states that directional coupling is the "conventional" method of data transmission in the art, there is clearly no suggestion or teaching in Osaka et al. of data transmission via data wiring as recited in Applicant's claims.

Therefore, for at least the reasons given above, Claims 1-64 are believed patentably distinct and allowable over the cited prior art reference. Accordingly, Applicant respectfully requests withdrawal of the rejection, with respect to Claims 1-64 under 35 U.S.C. §102(e).

CONCLUSIONS

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-64 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Applicant's undersigned attorney at the number indicated below.

Respectfully submitted,

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